Industry Pack Modules



IP480 Counter/Timer

IP480 modules provide up to six counter/timer channels for counting events, generating waveform control signals, measuring pulse-widths or periodic rates, and monitoring operations.

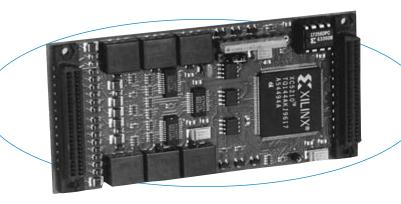
Support for internal or external triggering simplifies the synchronization of operations to specific events. Counter functions can use internally generated clocks or an externally supplied clock.



- IP480-6: Six 16-bit (three 32-bit) counter/timers IP480-2: Two 16-bit (one 32-bit) counter/timers
- Event counters
- Output waveform generator
 - continuous pulse
 - single pulse
 - continuous square waveforms
- Pulse-width or periodic rate monitor
- Watchdog timer with isolated relay output
- Interrupt support:
- watchdog timeout
- event count complete
- pulse-width or rate measurement complete
- pulse wave complete
- successive waveform generation
- Extended temperature option (-40 to 85°C)

Benefits

- Most configuration is handled by a single register which minimizes programming.
- Timer outputs support high voltage/currents.
- Built-in clamp diodes provide added protection when driving inductive loads.
- Pullups are socketed for easy adjustment.



The IP480 is very flexible and available in several varieties to accommodate a broad range of counter/timer applications.

Specifications

Counter/Timers

Counter/timer configuration:

IP480-6: Six 16-bit counter/timer function groups. IP480-2: Two 16-bit counter/timer function groups. Any two 16-bit counters may be combined together to create a 32-bit counter.

Speed (with 8MHz internal clock):

Max. output pulse/square wave freq.: 4MHz. Minimum event pulse width: 130nS. Minimum pulse width measurement: 250nS. Minimum period measurement: 250nS.

Mode accuracy (with external clocking):

Waveform generation: Period is ± 62 nS. Watchdog: Timeout occurs within ± 1 clock cycle. Pulse/period measurement: ± 1 clock cycle.

Internal clocks: Programmable 1, 4, or 8MHz.

External clocks: Separate clock input for each counter supports frequencies up to 7MHz.

Counter trigger: External inputs for triggering counter functions. Input level is TTL or CMOS compatible. Vih=2.0V, Vil=0.8V. Inputs are buffered and include 4.7K ohm pull-ups to +5V.

Input voltage range: 0 to 5V.

Input requirements: 2.0V DC minimum high level, 0.8V DC maximum low level, 10µA maximum current.

Output: Non-isolated open drains of N-channel mosfets with socketed 4.7K ohms pull-up resistor SIP. Drains protected to 60V DC and sink up to 250mA each.

Output range (low side switch): 0 to 5V with internal supply. 0 to 60V with pull-ups to external supply.

Output open drain pull-ups: A 4.7K ohms pull-up resistor SIP. Power limited to 0.15W/resistor.

Output relays:SPDT (Form C) electromechanical relays (one per counter) controlled in watchdog timer mode. Contacts rated to 125V AC, 1A.

IP Compliance (ANSI/VITA 4)

Meets all written IP specs per ANSI/VITA 4-1995.

IP data transfer cycle types supported: Input/output (IOSel*), ID read (IDSel*), Interrupt select (INTSel*).

Access times (8MHz clock):

Read/write cycles: 0 wait states (250ns cycle); 1 wait state (375nS cycle) to read the counter readback register.

Environmental

Operating temperature: 0 to 70°C (IP480-2/6) or -40 to 85°C (IP480-2E/6E).

Storage temperature: -55 to 125°C (all models).

Relative Humidity: 5 to 95% non-condensing.

MTBF: Consult factory.

Power: +5V (±5%): 255mA max. (-6), 110mA (-2). ±12V (±5%) from P1: 0mA max. (not used).

Ordering Information

Industry Pack Modules IP480-2

Two 16-bit (one 32-bit) counter/timers

IP480-2E

Same as IP480-2 plus extended temperature range

IP480-6

Six 16-bit (three 32-bit) counter/timers

IP480-6E

Same as IP480-6 plus extended temperature range For Industry Pack Carrier Cards, see Page 5.

Software (see Page 81)

IPSW-API-VXW

VxWorks® software support package

IPSW-API-QNX

QNX® software support package

IPSW-ATX-PCI

ActiveX*/OLE Controls 2.0 software package

IPSW-I INUX

Linux[™] support (website download only)

For accessories information, see Page 87.