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THE LEADER IN INDUSTRIAL I/O

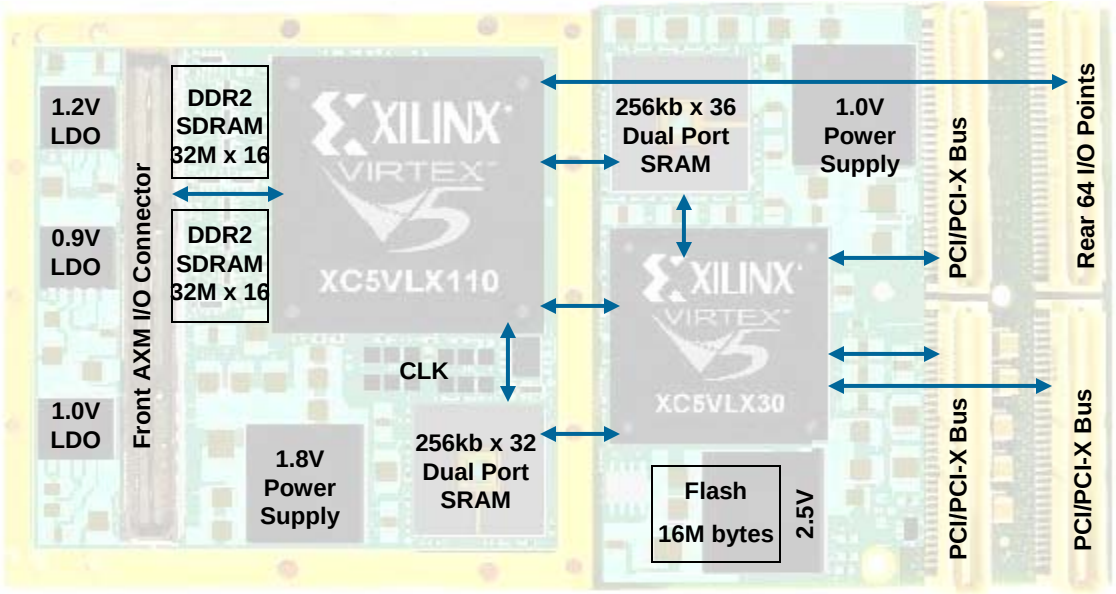
Dependable
Flexible
Compatible

PMC Virtex 5

Product Overview

PMC-Virtex 5 Overview

- Dependable
- Flexible
- Compatible



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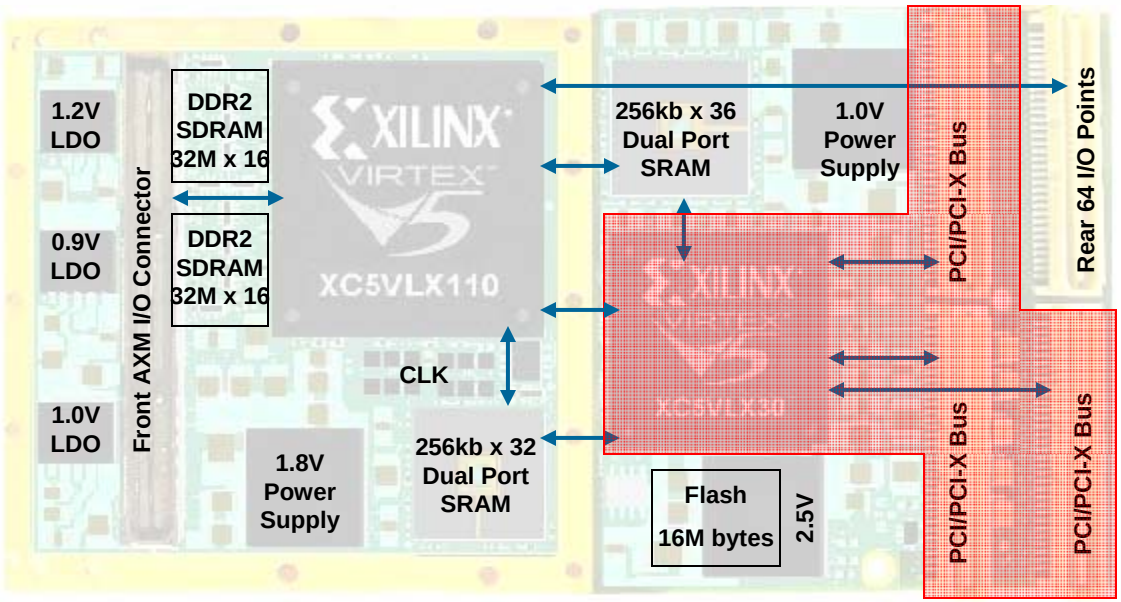
PCI Bus

Dependable
Flexible
Compatible

- 32 bit and 64-bit PCI-X Master/Target Interface
- Supports Bus Speeds up to 133MHz
- PCI r3.0 Compliant



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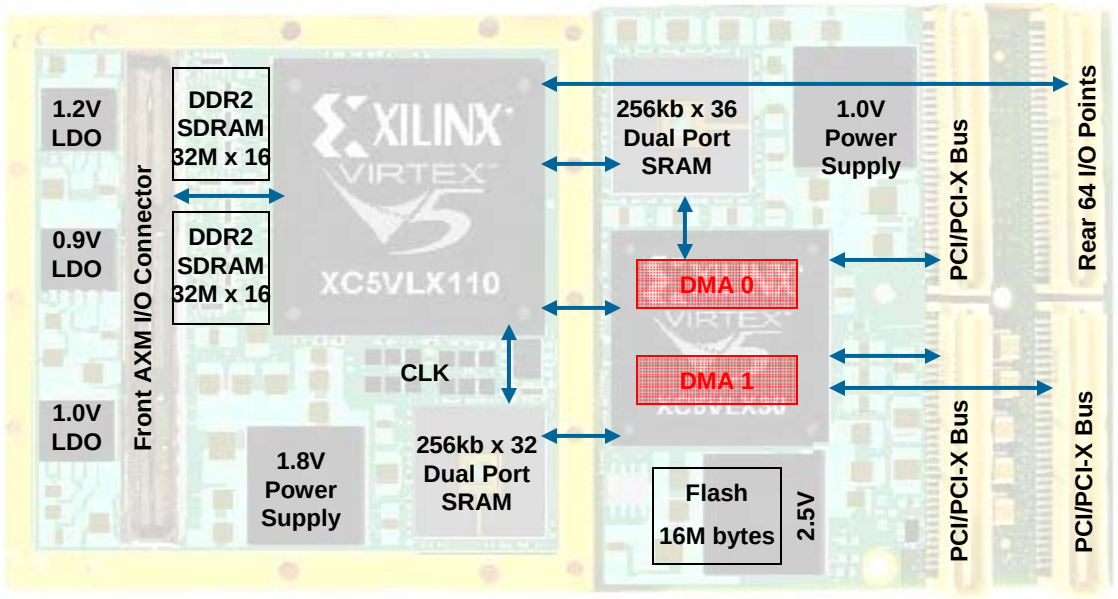
2 DMA Channels

- Block Mode
- Demand Mode
- Demonstrated 840 MB/sec Sustained Transfer Rate at 133MHz



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Virtex 5

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Compatible

- Device Resource Summary

Device	Logic Cells	DSP Slices	Block RAM	DCM	PLL
Virtex 5 LX110T	69,120	64	148	12	6
Virtex 4 LX60	59,904	64	160	8	0

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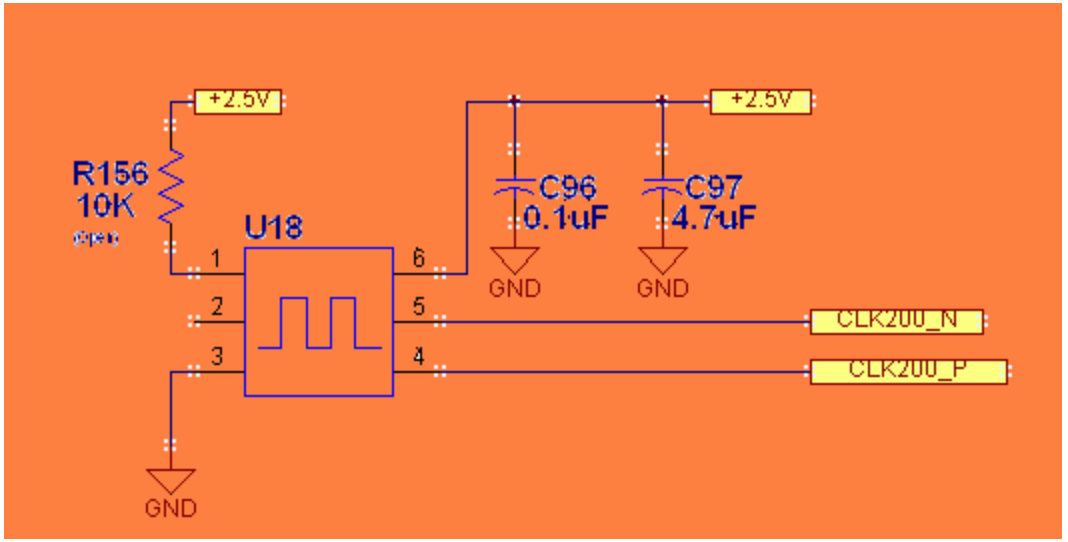
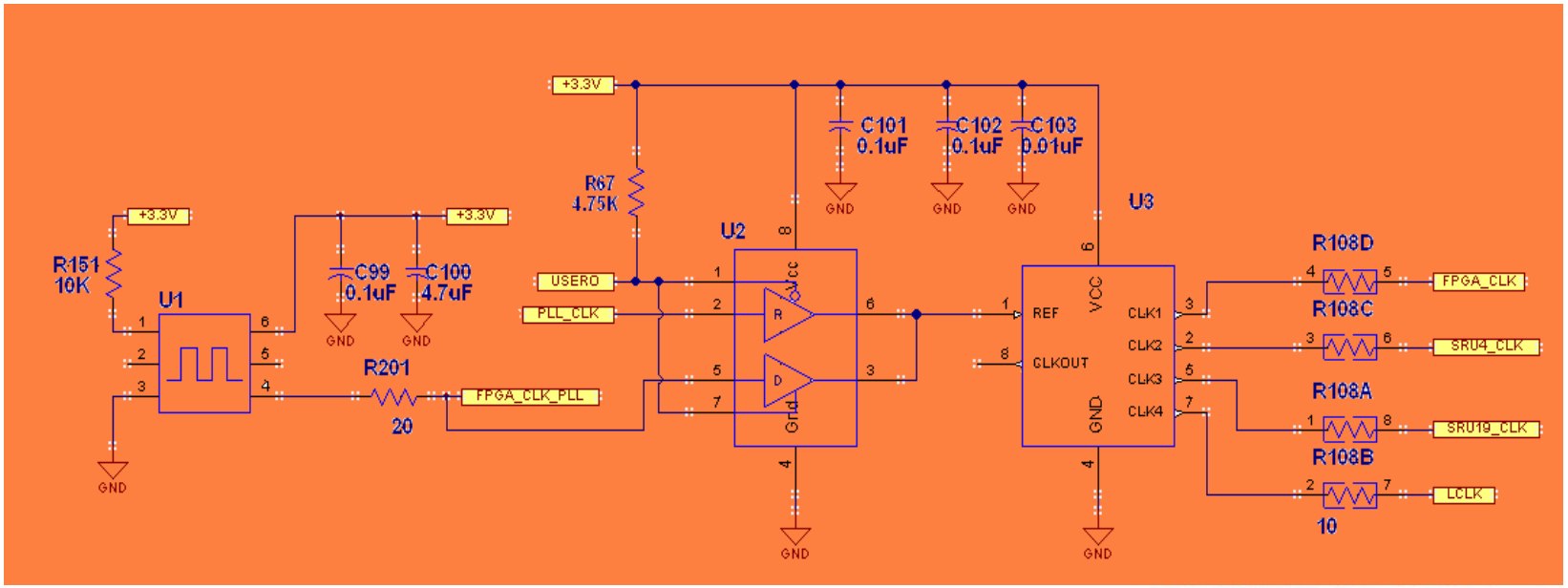
Board Clocks

- Dependable
- Flexible
- Compatible





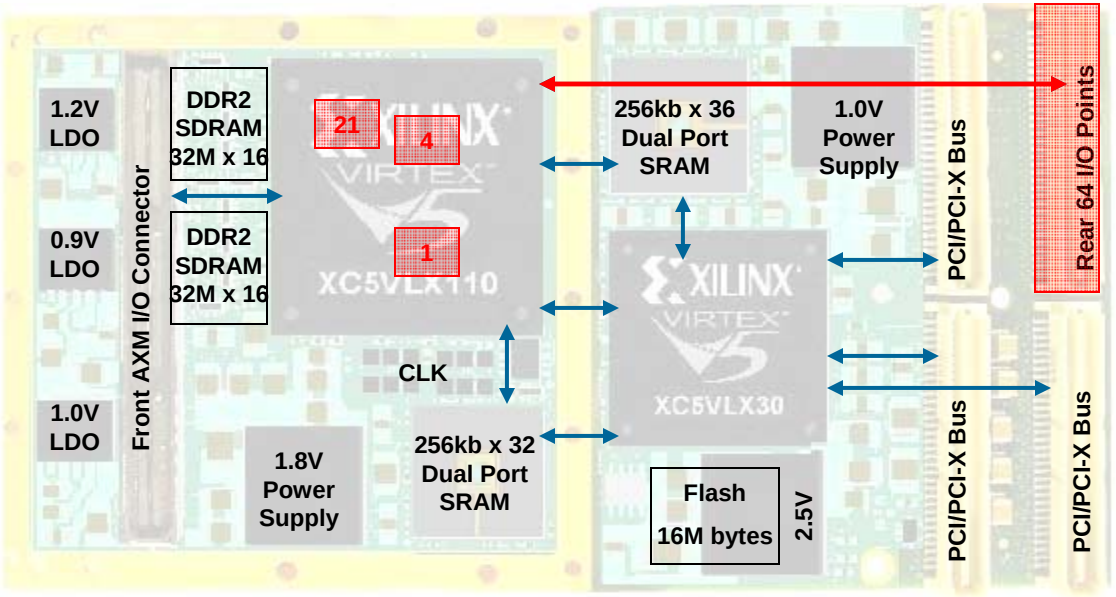
Rear Input/Output

Dependable

Flexible

Compatible

- Rear Input/Output via J4 Connector provides 64 I/O Points
- Link Directly to the Virtex 5 (banks 1,4, and 21)
- 8 Global Clock pins



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Dependable

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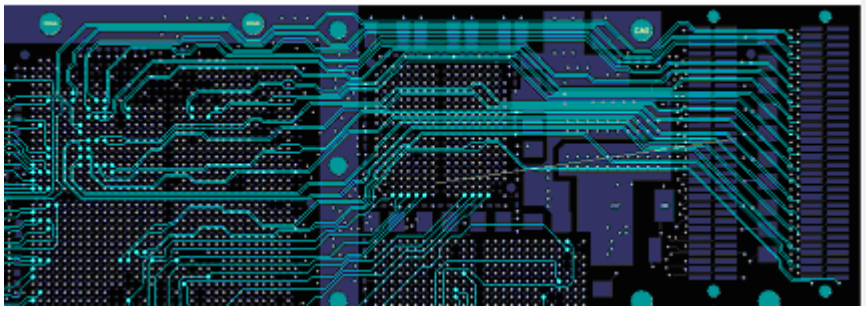
Rear Input/Output



- Supports 2.5 Volt IO Standards
- LVDS 1.25Vocm and .350VoDIFF
- Extended LVDS 1.25Vocm and 0.75VoDIFF
- HS Hypertransport 0.6Vocm and 0.6VoDIFF
- LVCMOS Voh min = 2.1v Vih min = 1.7v, Vol max 0.4v, Vil max 0.7v

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Front Mezzanine Connector

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Flexible

Compatible

- Samtex Connector Rated for 2GHz Operation
- Power Supplies Routed : +/-12, 5, 3.3, 2.5.
- Three Global Clocks from Bank 3 and 4
- Power to Bank 15 and 17 controlled by Mezzanine
  - VRN, VRP, and Vref from Bank 15 and 17
- JTAG Pins

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Front Mezzanine Connector

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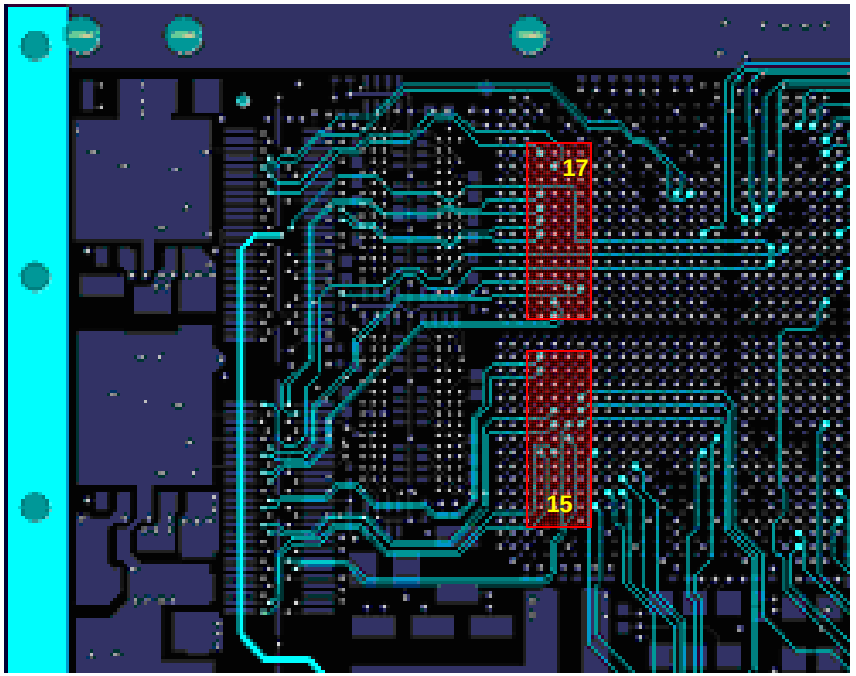
- I/O Signal Routed as Differential Pairs



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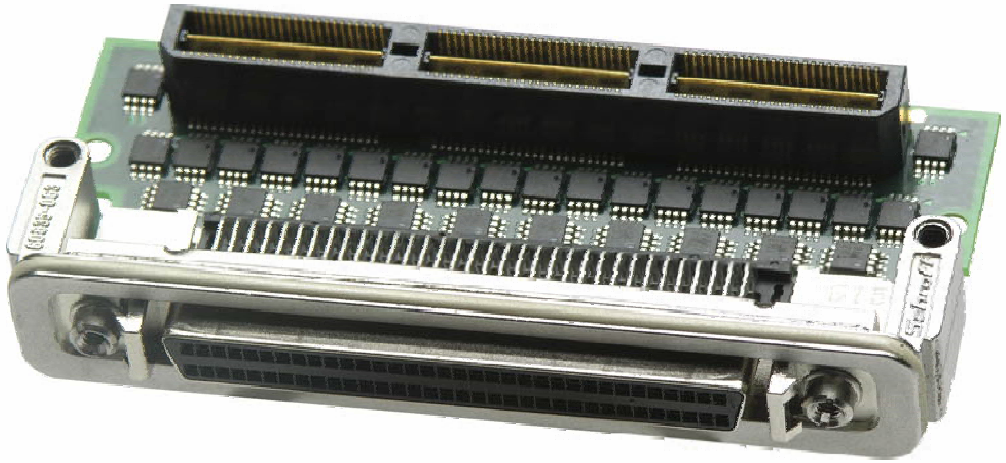
I/O Mezzanine Modules

Dependable

Flexible

Compatible

- AXM-DO2 30 Differential
- AXM-DO3 22 Differential 16 CMOS
- AXM-D04 30 LVDS
- AXM-A30 2 105MHz ADC
- AXM-EDK JTAG & LVTTL



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Dual Port Memory

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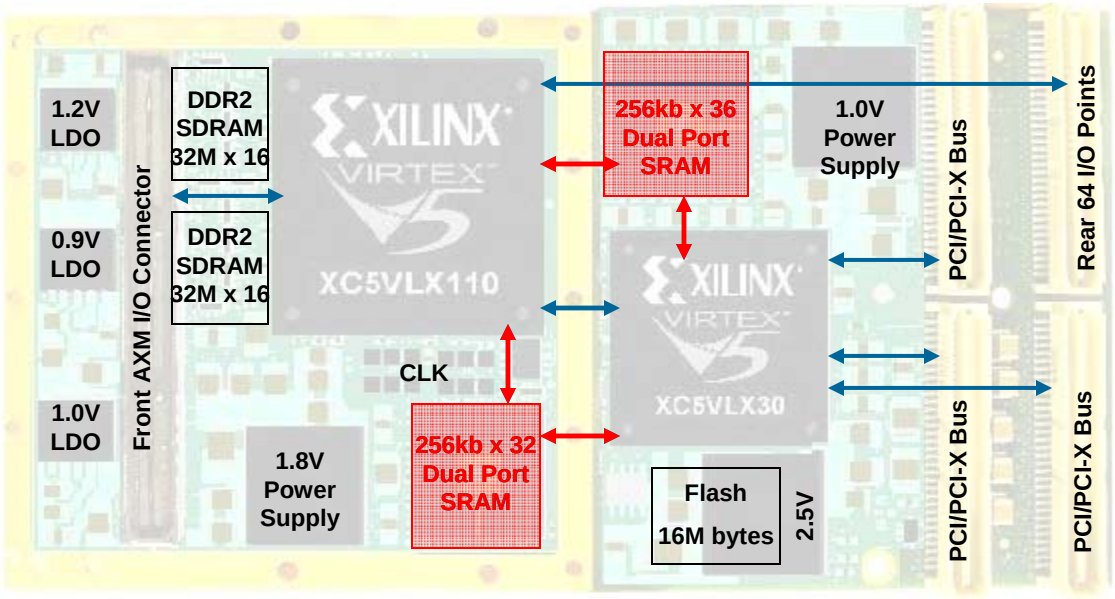
Compatible

- 256K x 64-bit
- Port to PCI bus and Port to FPGA
- Useful for DMA Transfer of Data
- Burst Transfers 840 MB/s



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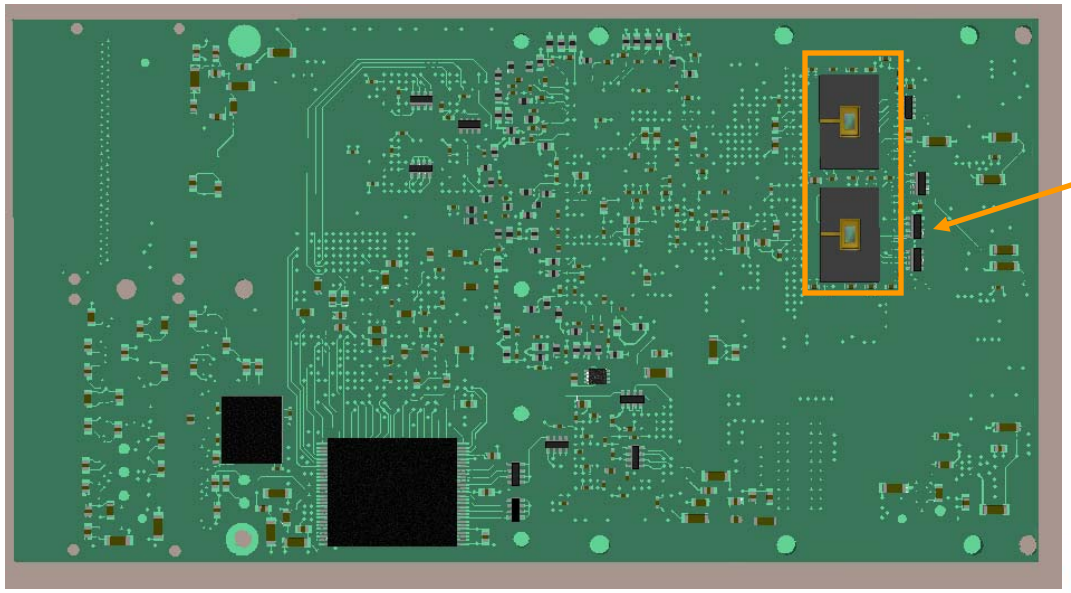
DDR2 SDRAM

- 32M x 32-bit
- Internal FPGA Controller Clock 150MHz
- Data Transfer Rate is 300M 32-bit words/s
- IP Provided by Xilinx Memory Interface Controller (MIG)



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Configuration Options

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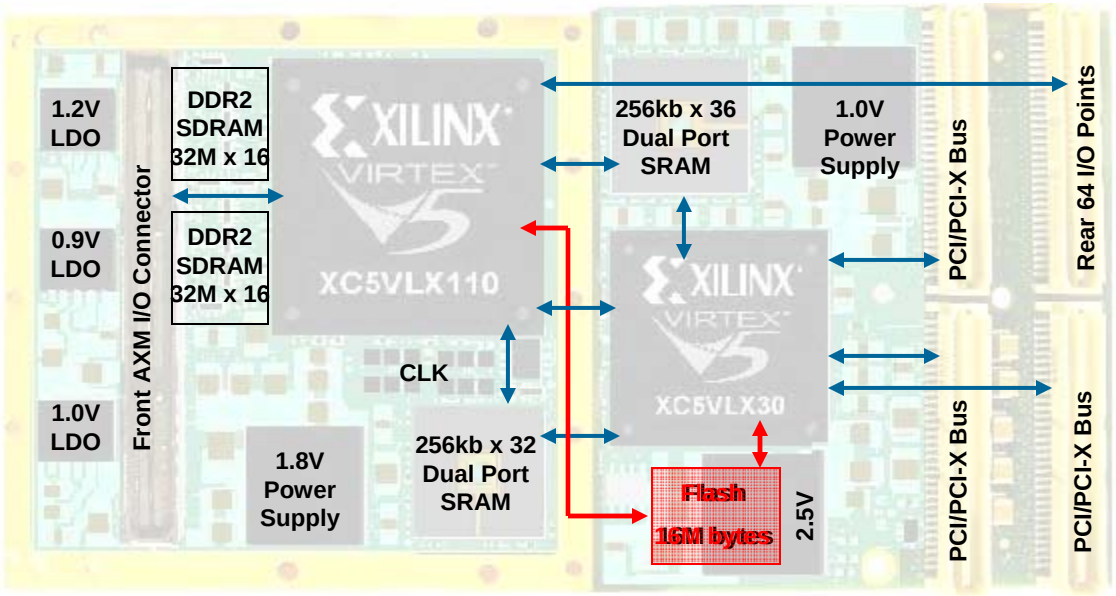
Compatible

- Automatic Configuration from Flash Memory on Power Up
  - Configuration starts after reset is released
  - Continues until FPGA DONE



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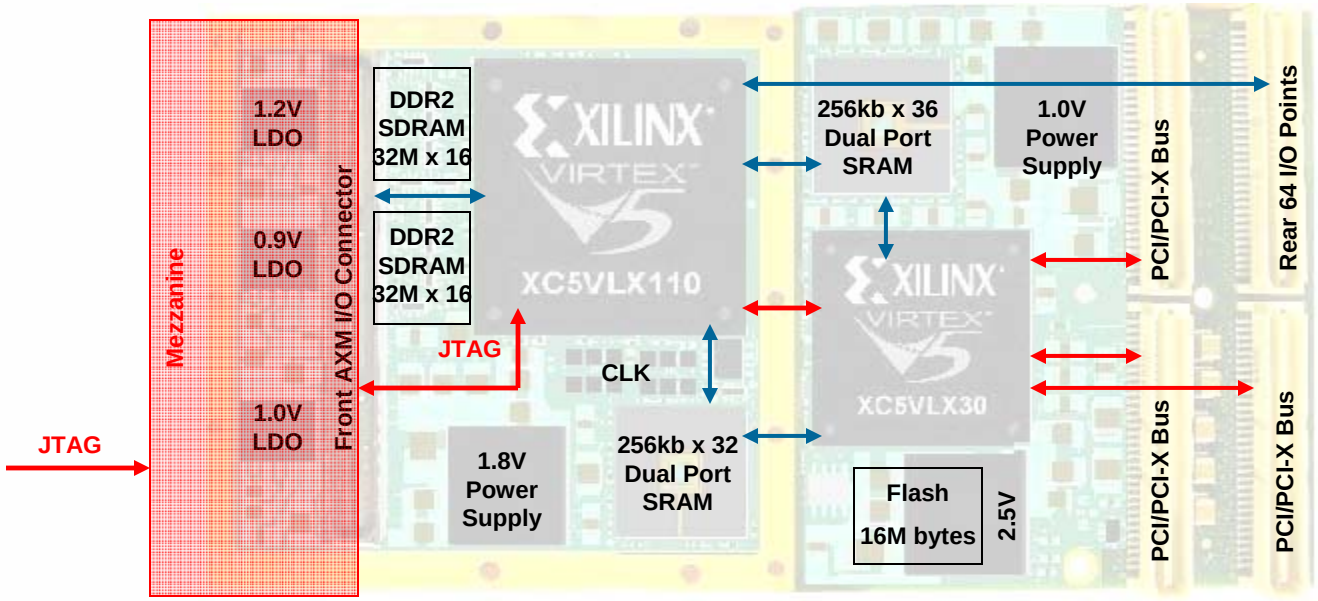
Configuration Options

Dependable

Flexible

Compatible

- Direct Over PCI Bus
  - 2.9 seconds LX40 FPGA Configuration Direct Time
- Front Mezzanine JTAG via EDK Board



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Flash Memory

- 16Mbyte Flash Device
  - On board Logic controls Flash Memory read and write operations
  - 128 addressable sectors
    - Each sector stores 128Kbytes
  - 31 sectors for LX110T
    - 3.9Mbyte Program Code Size

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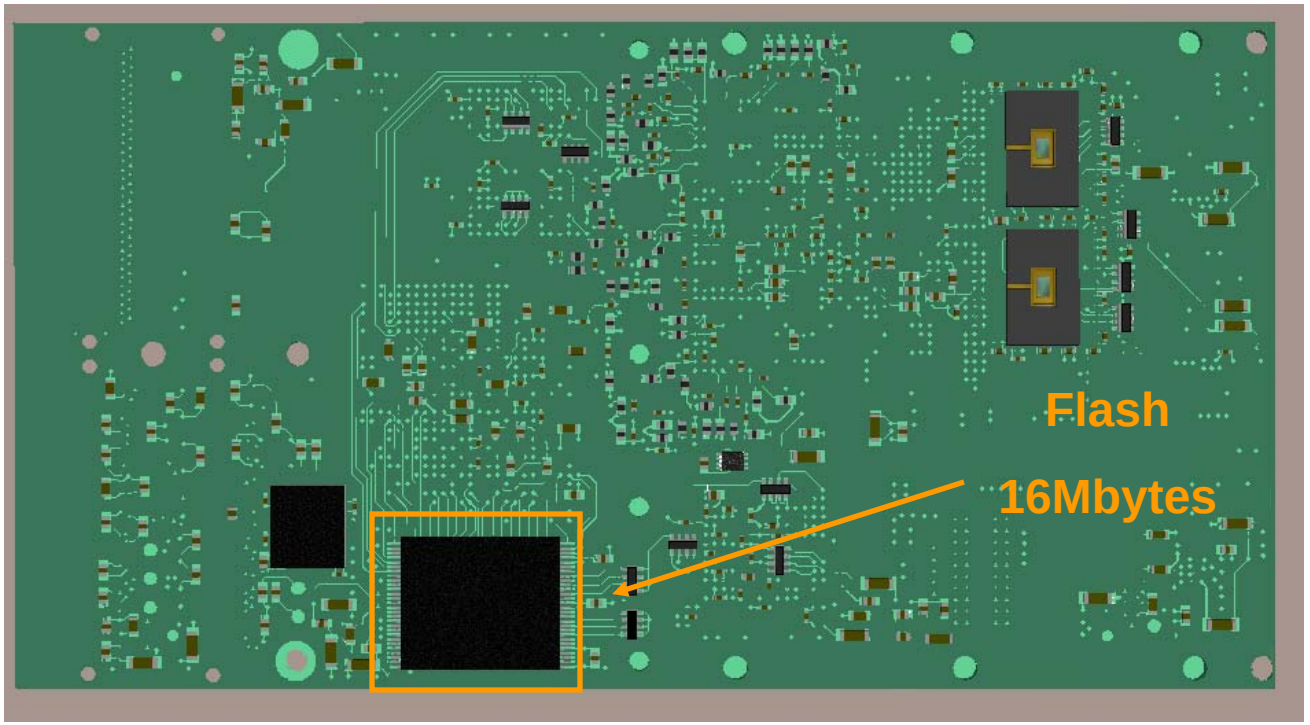
Flash Memory

Dependable

Flexible

Compatible

- 97 sectors remain user available
  - 12Mbyte User Flash space available



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EDK

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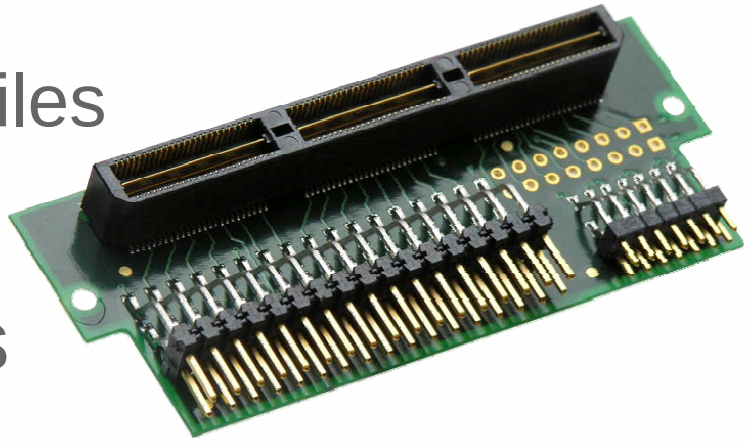
- User's Manuals
- New Getting Started Document
- Schematics
- VHDL
  - Example Design Files
- Constraint File
- Configuration Files



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