## IP231-x 16-Bit D/A, Analog Output

The IP231 outputs analog voltage signals to drive up to 16 devices. When used with a carrier that holds four IP modules, up to 64 voltage outputs can be obtained from a single card cage slot.

Each output channel has its own 16-bit D/A converter (DAC). Individual DACs are faster, and they eliminate glitches typically caused by the re-acquisition process of sample and holds found on multiplexed output boards.

Individual channels also have double-buffered data latches. You can select to update each output when it is written $t 0$, or to update all outputs simultaneously. Simultaneous outputs better simulate linear movements in motion processes.

## Features

- 8 or 16 analog voltage output channels
- Independent 16-bit D/A converters per channel with an $13 \mu S$ settling time
- Bipolar voltage (non-isolated) outputs: -10 to +10 volts
- Double-buffered DACs
- High load capability (5mA output current)
- Built-in calibration coefficients


## Benefits

- Outputs reset to 0 volts.
- Internally stored calibration coefficients ensure accuracy.
- Software provides easy selection of transparent or simultaneous output modes.
- Double-buffered DACs allow new data to be written to each channel before the simultaneous trigger updates the outputs.


The IP231 features individual D/A converters on each channel for better performance.

## Specifications

## Analog Outputs

Output configuration: 8 or 16 single-ended.
D/A Resolution: 16 bits.
Output range: Bipolar, -10 to +10 V .
Settling time: $13 \mu \mathrm{~S}$.
Maximum throughput rate:
Outputs can be updated simultaneously or individually. One channel: 13HS/conversion.
Sixteen channels simultaneously: $13 \mu \mathrm{~S} / 16$ channels.
System accuracy: $0.0305 \%$ of 20 V span maximum corrected error (i.e. calibrated) at $25^{\circ} \mathrm{C}$ with the output unloaded.
Linearity error: $\pm 2$ LSB (maximum).
Data format: Bipolar Offset Binary.
Output at reset: 0 volts.
Output current: - 5 to 5 mA (maximum). This corresponds to a minimum load resistance of 5 K ohms with a 10 V output.

## IP Compliance (ANSI/VITA 4)

Meets IP specifications per ANSI/VITA 4-1995.
IP data transfer cycle types supported:
Input/output (IOSe|*): DAC data, control registers, DAC offset and gain calibration coefficients.
ID read (IDSel*).
Access Times (8MHz clock):
ID EEPROM read: 0 wait states ( 250 nS cycle). DAC channel data write: 2 wait states ( 500 nS cycle). DAC offset/gain coeff. read: 1 wait state ( 375 ns cycle). Control register access: 1 wait state ( 375 nS cycle).

## Environmental

Operating temperature: 0 to $70^{\circ} \mathrm{C}$ (IP231-8/16) or - 40 to $85^{\circ} \mathrm{C}$ (IP231-8E/16E models).
Storage temperature: - 55 to $100^{\circ} \mathrm{C}$ (all models).
Relative humidity: 5 to $95 \%$ non-condensing
MTBF: $3,445,793$ hrs. at $25^{\circ}$ C, MIL-HDBK-217F, notice 2.
Power:
$+5 \mathrm{~V}: 45 \mathrm{~mA}$.
$+12 \mathrm{~V}: 200 \mathrm{~mA}$.
$-12 \mathrm{~V}: 180 \mathrm{~mA}$.

