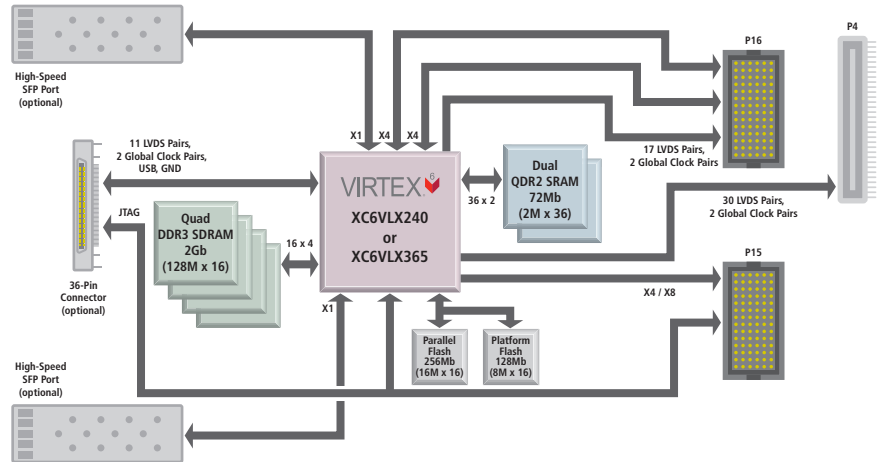
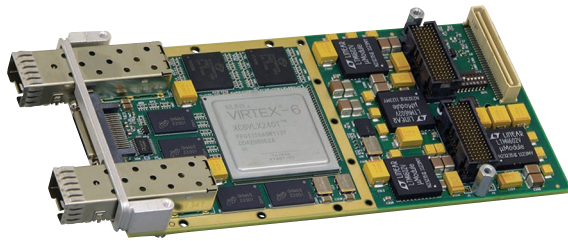


# XMC Modules

## XMC-6VLX User-Configurable Virtex-6 FPGA Modules

24 HOUR STOCK ITEM  
2 YEAR WARRANTY



VIRTEX<sup>6</sup>

### XMC module with PCIe and SRIO/Aurora interface ♦ Logic-optimized Virtex-6 FPGA ♦ Gigabit Ethernet

#### Description

Acromag's XMC-6VLX modules feature a high-performance user-configurable Xilinx® Virtex®-6 FPGA enhanced with high-speed memory and a high-throughput serial interface. The result is a powerful and flexible I/O processor module that is capable of executing custom instruction sets and algorithms.

The logic-optimized FPGA is well-suited for a broad range of applications. Typical uses include hardware simulation, communications, in-circuit diagnostics, military servers, signal intelligence, and image processing.

#### Two Versions: Rear I/O or Front + Rear

Two versions of this module are available, each offering a choice of an FPGA device with 240k or 365k logic cells. One version provides only rear I/O for use in air or conduction-cooled systems. The other version adds two SFP ports and a 36-pin connector on the front but only supports air-cooled systems.

On all versions, the rear I/O provides an 8-lane high-speed serial interfaces on both the P15 and P16 XMC ports for PCI Express, Serial RapidIO, 10-Gigabit Ethernet, or Xilinx Aurora implementation. P16 also supports 34 SelectIO channels. The P4 port adds another 60 SelectIO and global clock lines. SelectIO signals are Virtex-6 FPGA I/O pins that support single-ended I/O (LVCMOS, HSTL, SSTL) and differential I/O standards (LVDS, HT, LVPECL, BLVDS, HSTL, SSTL).

Models with front I/O add dual SFP ports and a VHDCR connector. The two SFP ports each provide a copper or fibre interface of up to 2.5Gbps. They also support a Gigabit Ethernet interface. The VHDCR connector interfaces JTAG, USB, and 22 SelectIO.

With Acromag's Virtex-6 FPGA modules, you can greatly increase DSP algorithm performance for faster throughput using multiple channels and parallel hardware architectures. Free up DSP processor CPU cycles by offloading algorithmic-intensive tasks to the FPGA co-processor.

These modules are ideal for high-performance customized embedded systems. Optimize your system performance by integrating high-speed programmable logic with the flexibility of software running on MicroBlaze™ soft processors.

Acromag's Engineering Design Kit provides software utilities and example VHDL code to simplify your program development and get you running quickly. A JTAG interface enables on-board VHDL debugging. Additional Xilinx tools help finish your system faster. Maximize FPGA performance with ISE® Design Suite. And with ChipScope™ Pro tools, you can rapidly debug logic and serial interfaces

#### Key Features & Benefits

- Reconfigurable Xilinx Virtex-6 FPGA with 240k or 365k logic cells
- 2M x 72-bit QDRII SRAM, 128M x 64-bit DDR3 SDRAM
- 16M x 16-bit parallel flash memory for MicroBlaze program code storage
- 128Mb platform flash memory to store power-up configuration bit file for Virtex-6 FPGA
- Dual 8-lane high-speed serial interfaces on rear P15 and P16 connectors for PCIe Gen 1/2, Serial RapidIO, 10Gb Ethernet, Xilinx Aurora
- Dual SFP ports for Fibre Channel or GbE
- 60 SelectIO or 30 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P4 port
- 34 SelectIO or 17 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P16 port
- 22 SelectIO, 2 global clock pairs, JTAG, USB, and ground signals via front 36-pin connector
- DMA support provides data transfer between system memory and the on-board memory
- Support for Xilinx ChipScope™ Pro interface
- Designed for conduction-cooled host card

Acromag   
THE LEADER IN INDUSTRIAL I/O

Tel 248-295-0310 ■ Fax 248-624-9234 ■ solutions@acromag.com ■ www.acromag.com ■ 30765 Wixom Rd, Wixom, MI 48393 USA

## XMC-6VLX User-Configurable Virtex-6 FPGA Modules

### Performance Specifications

#### ■ FPGA

##### FPGA device

Xilinx Virtex-6 FPGA.

Model XC6VLX240T FPGA with 241,152 logic cells and 768 DSP48E1 slices or Model XC6VLX365T with 364,032 logic cells and 576 DSP48E1 slices.

##### FPGA configuration

Download via JTAG or flash memory.

##### Example FPGA program

VHDL provided for bus interface, front & rear I/O control, SRAM read/write interface logic, and SDRAM memory interface controller. See EDK kit.

#### ■ I/O Processing

##### Front high-speed I/O

Two x1 lanes via SFP connectors for Gigabit Ethernet and Fibre Channel interface

##### Front user I/O

36-pin connector provides JTAG connection, USB signals, 2 global differential clock pairs, 11 LVDS signal pairs, and 2 ground signals.

##### Rear high-speed I/O

16 high-speed serial lanes.  
x8 lanes via P15 and x8 lanes via P16.

##### Rear user I/O

P16: 17 LVDS pairs (34 LVCMOS), 2 global clock pairs.  
P4: 30 LVDS pairs (60 LVCMOS), 2 global clock pairs.

#### ■ Engineering Design Kit

Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a XMC-6VLX module (see [www.acromag.com](http://www.acromag.com) for more information).

#### ■ XMC Compliance

Complies with ANSI/VITA 42.0 specification for XMC module mechanicals and connectors.

Complies with ANSI/VITA 42.3 specification for XMC modules with PCI Express interface.

Electrical/Mechanical Interface: Single-Width Module.

#### ■ Electrical

##### XMC PCIe bus interface (P15 and P16)

One 114-pin male connector (Samtec ASP-103614-05 or equivalent).

##### P15 primary XMC connector

8 differential pairs (Serial RapidIO, PCIe, 10-Gigabit Ethernet, or Xilinx Aurora). JTAG.

System Management (XMC provides hardware definition information read by an external controller using IPMI commands and I2C serial bus transactions.)

3.3V power: 4 pins at 1A/pin.

3.3V auxiliary power: 1 pin for system management.

Variable power (5V or 12V): 8 pins at 1A per pin.

##### P16 XMC connector

8 differential pairs (Serial RapidIO, PCIe, 10-Gigabit Ethernet, or Xilinx Aurora).

17 LVDS pairs or 34 SelectIO signals (differential pairs grouped per VITA 46.0 X38s).

2 global clock pairs.

Vcco pins are powered by 2.5V and support the 2.5V I/O standards.

##### P4 PMC rear I/O connector

64-pin female receptacle header (AMP 120527-1 or equivalent).

64 I/O connections (30 LVDS pairs plus two global clocks).

Vcco pins powered by 2.5V and support the 2.5V I/O standards.

##### VHDCR connector

36-position connector (Samtec VHDCR-36-01-M-RA) mates with industry-standard VHDCI cable assemblies.

##### SFP host connector (optional)

SFP transceiver signals route directly to Virtex-6 FPGA. 2.5Gb/s maximum data rate.

SFP copper (Gigabit Ethernet) or fibre optic modules available from Acromag.

#### ■ Environmental

##### Operating temperature

Standard models: 0 to 70°C.

##### Storage temperature

-55 to 125°C.

##### Relative humidity

5 to 95% non-condensing.

##### Power

3.3V (±5%): Application dependent.

12V (±5%): Application dependent.

##### MTBF

Contact the factory.

### Ordering Information

NOTE: XMC-6VLX-EDK is required to configure FPGA.

#### ■ XMC Modules

##### XMC-6VLX240

User-configurable Virtex-6 FPGA, 240k logic cells, no front I/O

##### XMC-6VLX240F

Same as XMC-6VLX240 plus SFP front I/O

##### XMC-6VLX365

User-configurable Virtex-6 FPGA, 365k logic cells, no front I/O

##### XMC-6VLX365F

Same as XMC-6VLX365 plus SFP front I/O

#### ■ Accessories

##### 5025-921

Cable, VHDCI 36-pin to SCSI-2, 6 feet long. Use with XMC-6VLX240F and XMC-6VLX365F.

##### 5028-449

Cable, copper twin-ax, SFP to SFP, 1 meter long.

##### 5028-455

Transceiver, 10/100/1000BASE-T copper SFP, up to 1.25Gb/s bi-directional data links.

##### 5028-452

Transceiver, short-wavelength SFP, up to 2.125Gb/s bi-directional data links.

#### ■ Software

For more information, see [www.acromag.com](http://www.acromag.com).

##### XMC-6VLX-EDK

Engineering Design Kit (one kit required)

##### PMCSW-API-VXW

VxWorks® software support package

##### PCISW-API-WIN

Windows® DLL software support package

##### PCISW-API-LNX

Linux™ support (website download only)

ISO9001  
AS9100



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